In the Claims

Please amend the claims as follows:

1. (Currently Amended) A method for emulation communications via a test data input port and boundary-scan architecture providing serial access to a serial connection of a plurality of registers disposed in a plurality of modules, each of the plurality of modules including at least one of the plurality of registers, comprising the steps of:

selecting for communication one of said plurality of modules, nonselected modules being nonresponsive to data on said serial connection;

supplying to the test data input port for communication to the boundary-scan architecture a serial signal having a number of bits greater in number than a number of bits of the serial connection of the plurality of registers, each bit of said serial signal having a first ~~logic~~ digital state;

following supply of said serial signal, supplying to the test data input port for communication to the boundary-scan architecture a single start bit having a second ~~logic~~ digital state opposite to said first ~~logic~~ digital state followed by a predetermined number of data bits;

at said selected module detecting said single start bit within the boundary-scan architecture and storing said predetermined number of data bits.

2. (Original) The method of claim 1, wherein:

said step of storing said predetermined number of data bits consists of storing said predetermined number of data bits in a program visible data register.

3. (Original) The method of claim 1, further comprising:

at said selected module, interpreting said predetermined number of data bits as an instruction and performing a function corresponding to said instruction.

4. (Currently Amended) The method of claim 1, wherein the boundary-scan architecture includes a test data output port following a last of the serial connection of registers, the method further comprising:

at said selected module, identifying a predetermined number of data bits to be transmitted, supplying a serial signal having said first ~~logic~~ digital state to following registers in the serial connection of the plurality of registers for a predetermined number of bits and supplying to following registers in the serial connection of the plurality of registers a single start bit having a second ~~logic~~ digital state opposite to said first ~~logic~~ digital state followed by said predetermined number of data bits.

5. (Currently Amended) The method of claim 1, wherein:

said first ~~logic~~ digital state is 1; and

said second ~~logic~~ digital state is 0.

6. (Currently Amended) A digital electronic module comprising:

a serial scan path having a serial input and a serial output and connecting through a plurality of data registers within the digital electronic module;

a start bit detector having a ~~serial~~ start bit detector input input, a ~~serial~~ start bit detector output and an alternative data output, said start bit detector monitoring serial data received at said ~~serial~~ start bit detector input and coupling serial data received at said ~~serial data~~ start bit detector input to said ~~serial data~~ start bit detector output except upon detection of a

number of serial bits greater than a first predetermined number having a first ~~logic~~ digital state followed by a single start bit having a second ~~logic~~ digital state opposite to said first ~~logic~~ digital state coupling a second predetermined number of bits of serial data received at said ~~serial data~~ start bit detector input to said alternative data output;

an alternative data input register connected to said alternative data output of said start bit detector for receiving and storing data output by said start bit detector on said alternative data output;

an input switch having a serial test data input and a mode input, said input switch connecting said serial test data input to said serial data input of said serial scan path upon receiving a ~~normal~~ serial scan path mode signal at said mode input and connecting said serial test data input to said serial data input of said start bit detector upon receiving an ~~alternative~~ alternate data transfer protocol mode signal at said mode input; and

an output switch having a test data output, said output switch connecting said serial data output of said serial scan path to said test data output upon receiving said ~~normal~~ serial scan path mode signal on said mode input and connecting said serial data output of said start bit detector to said test data output upon receiving said ~~alternative~~ alternate data transfer protocol mode signal at said mode input.

7. (Currently Amended) The digital electronic module of claim 6, wherein:

said first ~~logic~~ digital state is 1; and

said second ~~logic~~ digital state is 0.

8. (Previously Added) The digital electronic module of claim 6, further comprising:

a bypass path connecting said input switch and said output switch;

said input switch further connecting said serial test data input to said bypass path upon receiving a bypass path mode signal at said mode input; and

said output switch further connecting said bypass path to said test data output upon receiving said bypass path mode signal at said mode input.

9. (Previously Added) The digital electronic module of claim 6, further comprising:

a digital circuit connected to said alternative data input register operable to employ data stored in said alternative data input register.

10. (Previously Added) The digital electronic module of claim 9, wherein:

said digital circuit includes a programmable digital processor core.

11. (Previously Added) The digital electronic module of claim 10, wherein:

said programmable digital processor core employs data stored in said alternative data input register as an instruction controlling execution by said programmable digital processor core.

12. (Currently Amended) The digital electronic module of claim 9, further comprising:

an alternative data output register connected to said digital circuit storing data specified by said digital circuit;

a start bit generator connected to said alternative data output register and said output switch, said start bit generator

generating a serial signal having a predetermined number of bits, each bit of said serial signal having a first ~~logic~~ digital state, generating a start bit having said second ~~logic~~ digital state followed by data stored in said alternative data output register; and

said output switch further connecting said serial signal, said start bit and said data stored in said alternative data output register to said test data output.